



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,882	01/21/2004	Erik Heinemann	20046/0200734-US0	5436

7278 7590 02/04/2005

DARBY & DARBY P.C.  
P. O. BOX 5257  
NEW YORK, NY 10150-5257

EXAMINER
----------

BUI, HUNG S

ART UNIT	PAPER NUMBER
----------	--------------

2841

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

<b>Office Action Summary</b>	<b>Application No.</b> 10/762,882	<b>Applicant(s)</b> HEINEMANN ET AL.	
	<b>Examiner</b> Hung S. Bui	<b>Art Unit</b> 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 January 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>01/21/04</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-9 and 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gogami et al. [US 6,076,737] in view of Takahashi [US 6,031,724].

Regarding claims 1-2 and 13, Gogami et al. disclose a chip card (figure 1b) comprising:

- a chip card body (2) having a first cavity (a volume to hold a carrier substrate 11) and a second cavity (3), wherein the second cavity is recessed into a base of the first cavity (figure 1b), so that the first cavity extends laterally beyond the second cavity and a base surface of the first cavity surrounds the second cavity;
- a carrier substrate (11) secured to the chip card body and arranged in the first cavity, wherein the carrier substrate has an upper surface contact (15) for reading the chip card on its top side and a lower surface contact (16) on its underside, which are electrically connected to one another by contact-hole lines (19, column 4, lines 36-40) which run through the carrier substrate, the contact hole-lines passing through both the lower surface contacts and the upper surface contacts and being arranged in a region of the first cavity which

Art Unit: 2841

extends laterally outside the second cavity, and the contact-holes being covered at the base of the first cavity (figure 1b);

- a semiconductor chip (12) connected to the lower surface contacts of the carrier substrate by electrical connections and provided in the second cavity.

Gogami et al. disclose the instant claimed invention except for a bonding layer, which extends from the base of the first cavity into an interior of the second cavity and covers a region of the semiconductor chip, securing the carrier substrate, on its underside, to the base surface of the first cavity.

Takahashi discloses an IC chip card (figures 1-2) having a card body (13) and a substrate (11a) including a chip (11b) mounted therein, wherein the card body has first cavity and a second cavity extending downward from the first cavity (figure 1), wherein the first and second cavities have a bonding layer (16), which extends from the base of the first cavity into an interior of the second cavity and covers a region of the chip (11b), securing the carrier to the carrier substrate, on its underside, to the base surface of the first cavity (figure 1).

It would have been obvious to a person having ordinary skill in the art at the time invention was made to use the bonding layer design of Takahashi with the chip card of Gogami et al., in order to secure and protect the chip in the cavities.

Regarding claim 3, Gogami et al. disclose an anisotropic conductive paste (18) covering the semiconductor chip in a region of the electrical connections to the lower surface contacts of the carrier substrate, and not covering a region of the semiconductor chip which is not covered by the paste.

Art Unit: 2841

Regarding claims 4-5 and 14, Gogami et al., as modified, disclose the instant claimed invention except for the bonding layer covering the contact hole-lines.

It is well known in the art to mount a chip on a carrier by using an adhesive bonding layer. Takahashi discloses a chip mounted on a carrier using a bonding layer from the first cavity down to the second cavity and sealing the chip. The bonding layer design of Takahashi can be applied to mount the carrier substrate design with the hole-line of Gogami et al. in its card body.

It would have been obvious to a person having ordinary skill in the art at the time invention was made to mount the chip on the chip card body of Gogami et al. by using the bonding layer design of Takahashi, for the purpose of completely sealing the chip in the cavities of the card body.

Regarding claims 6 and 15, Gogami et al. disclose the lower surface contact (16,) of the carrier substrate extends beyond an inner edge of a base surface of the first cavity and above the semiconductor chip within the second cavity (figure 1b).

Regarding claims 7 and 16, Gogami et al. in view of Takashi disclose the semiconductor chip being bonded to the lower surface contacts of the carrier substrate using a flip-chip method (column 1, lines 28-39).

It would have been obvious to a person having ordinary skill in the art at the time invention was made to mount the chip onto the substrate of Gogami et al. by using a flip chip method, as suggested by Takahashi, for the purpose of reducing manufacturing cost.

Art Unit: 2841

Regarding claims 8 and 17, Gogami et al., as modified, disclose the instant claimed invention except for the use of a material that only becomes adhesive at an elevated temperature.

It would have been obvious to a person having ordinary skill in the art at the time invention was made to use a material that only becomes adhesive at an elevated temperature to make the chip card of Gogami et al., as modified, for the purpose of mounting/aligning the semiconductor chip in the chip card.

Regarding claims 9 and 18, Gogami et al. disclose the instant claimed invention except for the bonding layer being formed of a cured liquid adhesive.

Takahashi discloses the bonding layer being formed of a liquid adhesive (column 4, lines 21-35).

It would have been obvious to a person having ordinary skill in the art at the time invention was made to use the liquid adhesive of Takahashi for bonding the chip of Gogami et al., for the purpose of reducing deformation/leakage during the manufacturing process.

3. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gogami et al., as modified, as applied to claims 9 and 18 above, and further in view of Fidalgo [US 5,671,525].

Regarding claims 10 and 19, Gogami et al., as modified, disclose the instant claimed invention except for the bonding layer being formed of cured cyanoacrylate.

Art Unit: 2841

Fidalgo disclose a chip card (1, figure 1) having a chip (8) mounted on a substrate (3) by using a cyanocrylate adhesive (column 5, lines 57-67).

It would have been obvious to a person having ordinary skill in the art at the time invention was made to use a cyanocrylate adhesive to mount a chip on its chip card body of Gogami et al., as modified, for the purpose of rapidly securing the chip to the substrate.

4. Claims 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gogami et al., as modified, as applied to claims 1 and 12 above, and further in view of Berney [US 6,491,229].

Regarding claims 11 and 20, Gogami et al., as modified, disclose the instant claimed invention except for the chip card being used for a mobile radio card.

Berney discloses a chip card (figure 1) being used for a radio card (see abstract).

It would have been obvious to a person having ordinary skill in the art at the time invention was made to use the chip card of Gogami et al., as modified, as a mobile radio card, as suggested by Berney, for the purpose of hands free access card.

### ***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung S. Bui whose telephone number is (571) 272-2102. The examiner can normally be reached on Monday-Friday 8:30AM-6:00PM.

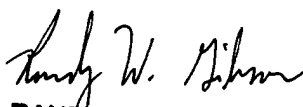
Art Unit: 2841

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/25/05

HB

  
RANDY W. GIBSON  
PRIMARY EXAMINER